

### Fourth-generation performance and economy

### Hardware

The state-of-the-art semiconductor technology used throughout the central processing units and channel processors (CHPs) makes possible a high internal speed of 700-picosecond (trillionths of a second) propagation delay per gate and 31.5 nanosecond CPU cycle time. In addition, it substantially reduces the number of components and interconnections, thus contributing to improved reliability.

The high-speed buffer with a cycle time of 31.5 nanoseconds and a capacity of 32,768 bytes upgrades CPU performance.

Efficient virtual storage control is made possible by a CPU dynamic address translation (CPU DAT) facility and a channel dynamic address translation (channel DAT) facility. The channel DAT is designed to reduce control program overheads related to channel command program management in the virtual storage environment. For example, the number of steps for channel program management has been decreased as much as 30 to 40 percent compared with that without the channel DAT.

The multiprocessing feature offers a cost-effective improvement in availability and throughput.

The addition of the service processor (SVP) dedicated to console functions provides extensive services to operators, logging of hardware errors, and diagnosis of CPU malfunctions.

The channel processor executes channel command programs. Its features include channel DAT and control of 16 channels.

The communication control processors (CCPs) are the front-end processors for the data communications control. The network control program (NCP) they execute greatly improves online system flexibility and throughput.

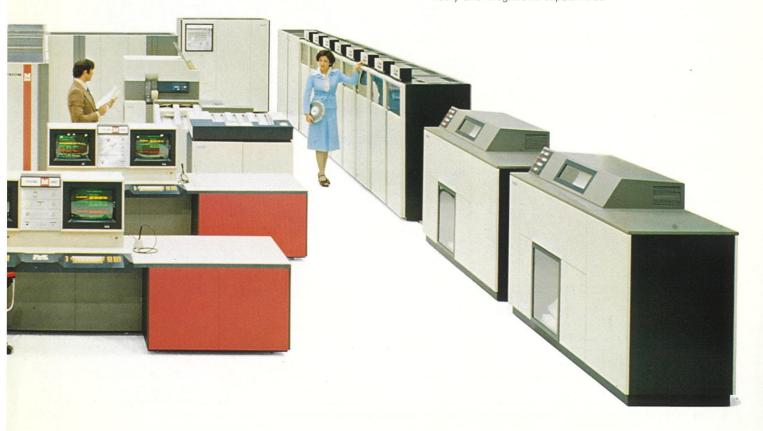
The instruction set of 193 includes ten special instructions designed to enhance arithmetic and system control functions.

A wide range of cost-effective and easy-to-operate peripherals and terminals is available. For example, disk pack drive units—the FACOM 479B2 with two spindles of 200-million-byte capacity each and the FACOM 493A2/B2/C2 with two spindles of 317-million-byte capacity—are very suitable for data base systems.

The disk pack cross-call adapter (DPXA) provides a device cross-call function, thus improving system reliability and availability.

Installation costs have been substantially reduced thanks to the smaller size made possible by the use of LSI semi-conductor technology and the advanced 100% air cooling system that eliminates the need for cooling pipes.

Reliability, availability, serviceability (RAS) features include error checking and correction (ECC), instruction retry and diagnostic capabilities.



# Advanced functions for improved productivity

### **Operating system**

### OSIV/F4

OSIV/F4 is the top-performance operating system for medium- to very large-scale systems of the M-series. Its multiple virtual storage feature provides each system user with a private address space of 16 million bytes. This feature relieves programmers of the burdens imposed by complicated techniques such as dynamic overlays and excessive job steps. The freedom from storage space limitations greatly facilitates smooth system growth.

The advanced information manager (AIM) provides users with versatile data base (DB) and data communication (DC) capabilities.

The time sharing system (TSS) allows the user to make use of the computer from a terminal. Its features include compatibility with batch environment; conversational remote job entry function; enhancement of debugging functions with the aid of TEST command, syntax checkers, interactive debug functions and EDIT command; user protection and failure localization based upon the multiple virtual storage concept.

Powerful job scheduling and data management services are provided. The job entry subsystem (JES) contributes to the efficiency of job management by spooling and scheduling input and output streams. Remote entry services (RES) give full access to batch processing services from remotely located terminals.

The automatic priority group (APG) facility attempts to balance CPU-limited jobs and I/O-limited jobs by periodically modifying the dispatching priority.

System decision manager (SDM) and virtual I/O (VIO) permit full exploitation of multiple virtual storage capabilities and system resources. SDM can operate under multiple modes including batch, remote-batch, time sharing, and real time online processing.

The virtual storage access method (VSAM) offers an efficient access method for sequential and direct processing by means of an index key or relative byte address.

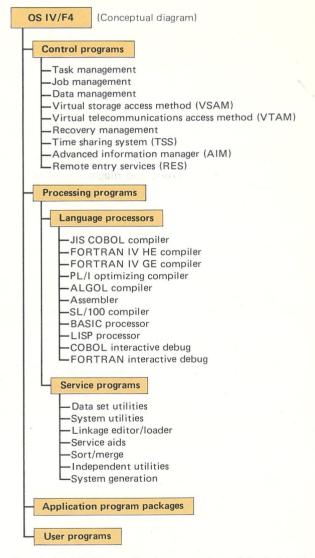
VSAM provides device-independent data sets for long-term stability. Most of the VSAM data set attributes are collected into the VSAM catalog. Passwords can be created at four different levels to safeguard data sets.

The virtual telecommunications access method (VTAM) facilitates communication between application programs and terminals. VTAM provides an efficient management of network resources.

Multiple console support smooths the communication flow between operators and the operating system. Color displays on the consoles facilitate message recognition. Automatic volume recognition (AVR) permits operators to premount volumes on any available disk pack drive units or magnetic tape units.

The system management facilities (SMF) collect information such as user accounting records, data set activity records, volume records, and system records.

The patrol diagnosis program (PADIA), recovery management system (RMS), functional recovery routine (FRR), online test program (OLTE), and teleprocessing online test program (TOLTE) greatly enhance the OSIV/F4 operating system's RAS capabilities.



- Note 1: JIS COBOL specifications cover those of OS Full ANS COBOL version 3.
- Note 2: FORTRAN IV HE specifications cover those of OS FORTRAN IV (H extended).
- Note 3: FORTRAN IV GE specifications cover those of OS FORTRAN IV (G1) and of Code and Go FORTRAN.
- Note 4: ALGOL specifications comply with ISO recommendations except for input/output procedures.

#### LSI technology

Size of LSI chip	4mm x 4mm
Type of technology	Bipolar emitter-coupled logic
Propagation delay per gate (on the LSI chip)	700 picoseconds (*)
Maximum number of gates per chip	100

(\*) one picosecond is one trillionth  $(10^{-12})$  of a second.

#### Central processing unit

Number of CPUs per system	1 (Uniprocessing system) 2 (Multiprocessing system)
Cycle time	31.5 nanoseconds
Instruction set	193
General purpose registers	16 (32 bits per register)
Floating-point registers	4 (64 bits per register)
Control registers	16 (32 bits per register)
Data formats	Byte (8 bits) Halfword (16 bits) Fullword (32 bits) Double precision word (64 bits) Extended precision word (128 bits)
Dynamic address translation	Translation lookaside buffer (256 entries) Segment table origin stack (32 entries)
Timers	CPU timer Time-of-day clock Clock comparator Interval timer

#### High-speed buffer

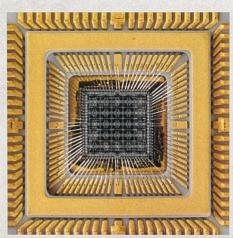
Technology	Bipolar integrated circuit
Cycle time	1 CPU cycle
Capacity	32,768 bytes

#### Main storage unit

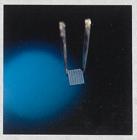
Technology	N-channel metal oxide semiconductor
Minimum storage capacity	1,048,576 bytes
Maximum storage capacity	16,777,216 bytes
Cycle time	16 CPU cycles per 32 bytes
Interleaving	2 ways or 4 ways
Error checking and correction	Correction of all single-bit errors, detection of all double-bit errors and some multiple-bit errors

#### Channel processors

Number of channel processors per CPU	1 or 2
Number of channels per CPU	Maximum 16
Types of channels	Byte multiplexer channel Block multiplexer channel Selector channel
Throughput	12 megabytes per second (one CHP) 20 megabytes per second (two CHPs)
Channel DAT facility	With







Left: LSI chip (actual size)

Above left: LSI chip mounted in a chip carrier Above: LSI chip carriers, with cooling stud

LSI chip carriers, with cooling studs and fins attached, mounted on

multichip carrier (multiple layer printed circuit board)

The information contained in this brochure is primarily of an introductory nature. Specifications are subject to change without notice, and some equipment, devices, options and programs described herein may not be available in every locale. For the latest information, including specifications, availability and delivery schedules, contact your local Fujitsu representative.

Forth edition, February 1979

# FUJITSU LIMITED

Communications and Electronics